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VHF SILICON POWER TRANSISTOR

Report No. 2

Contract No. DA 36-039 SC 90837

DA Project No. 3A99-21-001

Period covered

Second Quarterly Report

1 October 1962 to 1 January 1963

U. S. Army Signal Research and Development Laboratories

U. S. Army Signal Supply Agency

Fort Monmouth, New Jersey

Shockley Transistor
Unit of Clevite Transistor
Stanford Industrial Park
Palo Alto, California

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Report Edited by

R. M. Scarlett

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1. PURPOSE

It is the purpose of this work to design and fabricate experimental high frequency power transistors capable of delivering 50 watts of power at 150 Mc and meeting the other requirements of SCL-7002/115, and to produce 200 units of the final model.

2. ABSTRACT

The continued development of the 50 watt VHF silicon power transistor in the areas of diffusion, metallizing and packaging is described. The theory of lateral thermal instability is discussed. This instability is fundamental to all transistors, and leads to the development of hot spots and consequent secondary breakdown. It severely limits the power capability of large-area devices. Means are proposed to substantially raise the power level at which the instability occurs. Initial experiments in making stabilized devices employing either epitaxially grown resistive emitter layers, or lumped emitter resistors are reported.

Experimental devices show the expected small-signal properties ($f_t \simeq f_{max} \simeq 450$ Mc), but the large-signal performance is still poor due to insufficiently thick metal contacts and the influence of the wide backbone region.

3. PUBLICATIONS, LECTURES, REPORTS AND CONFERENCES

Monthly performance summaries and one Quarterly Report covering July 1 - October 1, 1962 have been submitted to the contracting officer as required. Six experimental model transistors were submitted on 1 November 1962.

4. FACTUAL DATA

4.1 Diffusion

4.1.1 Diffusion Schedules

Two different diffusion schedules, one leading to a device having all the junctions close to the surface, the other to one with somewhat deeper diffusions, were evaluated. Both structures had a base layer thickness of $0.8 \pm 0.1\mu$. The thin devices had the emitter junction 1μ below the surface, versus 2μ for the thicker ones. From the viewpoint of diffusion control it could be expected that the structures with the shallow junctions should have a better yield because the base width is 45% of the total thickness versus 29% for the deeper junctions. Therefore, the chance for the occurrence of shorts through the base layer is much higher in the latter case. In spite of this the yield of good devices after diffusion was around 50% for the shallow structures and around 70% for the deep structures. Most of the rejection was not due to emitter-collector shorts but to soft collector base characteristics.

The explanation for the difference in yield seems to be as follows: the shallow emitter diffusion was only 5 minutes at 1050 °C compared to 20-30 minutes for the deeper diffusion. Since the emitter diffusion is carried out in the presence of P_2O_5 vapors, there is gettering action[1] that has the effect of hardening the collector base characteristic by the removal of metal precipitates. The diffusion time for the shallow emitter is too short to permit effective gettering.

A further benefit of the deeper diffusion is improved current gain (β) at currents above 2 amperes due to the higher emitter efficiency produced by the thicker emitter layer.

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1. A. Goetzberger and W. Shockley, J. Appl. Phys. 31, 1821 (1960).

4.1.2. Impurity Distribution in the Base Layer

It has been noted recently that steam oxidation of silicon causes depletion of boron in surface layers close to the growing oxide. It is conjectured that the high affinity of steam grown oxide for boron is the reason for this effect. Therefore, the question arose whether during the base layer diffusion in steam the boron surface concentration is depressed more than expected from diffusion laws. If this were the case, an unnecessary increase of base resistance would occur. A determination of the impurity concentration profile after base diffusion was therefore carried out using the anodic oxidation technique[2].

The result is shown in Fig. 1. The curve starts from a low value at the surface, reaches a maximum at 0.25μ, and follows a Gaussian distribution to about a 2μ depth. At larger depths, the concentration drops faster than the Gaussian curve, leading to a thinner layer than would be expected.

The shape of the impurity distribution curve of Fig. 1 can be partly understood on the basis of a model in which the boron predeposited layer is steam oxidized in the initial stages of the diffusion, and this thin oxide layer tends to retain the boron[3]. The physical picture is that of a thin film at the surface, having a higher concentration of boron than in the silicon, and losing boron atoms by diffusion into the silicon and by outdiffusion. A segregation coefficient is introduced in the theory, describing the boron concentration at the silicon surface compared to that in the oxide. The experimental data indicates that this segregation coefficient is of the order of 0.16.

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2. E. Tannenbaum, Solid State Electronics 2, 123 (1961).

3. H. Strack, unpublished memorandum.

4.1.3. Surface Passivation

As outlined in the first quarterly report, a mesa structure is used for the present power transistor because large area planar devices have lower yields. In order to passivate the collector base junction, oxide has to be applied after etching. Anodic oxidation and subsequent thermal annealing was found to be adequate, but the oxide cover was rather thin which sometimes resulted in damage during mounting and encapsulation. A new technique giving thicker oxide layers is presently being evaluated. Silicon dioxide is deposited on the freshly etched junctions by pyrolytic deposition of ethyl silicate at 700°C in vacuum[4]. No degradation of junction characteristics was found after decomposition of 0.6 μ of oxide.

The growth rate is approximately 0.4 μ /h. Subsequent heat treatment of devices coated in this manner revealed that they can be exposed to temperatures up to 700°C without deterioration. At higher temperatures a reduction of breakdown voltage could be observed. A group of the devices has been canned and is presently undergoing storage at 300°C to determine long term stability.

4.2 Metallizing

In the first quarterly report, the desirability of having thick aluminum contacts on the emitter and base regions was pointed out. For the particular geometry employed, with 32 emitter fingers each having an aluminum contact 25 μ wide and 560 μ long, minimum aluminum thickness of 2.5 μ was calculated to avoid excessive voltage drop ($> kT/q$) along a

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4. J. E. Sandor, Paper given at the Los Angeles Meeting of the Electrochem. Soc. 1962.

finger. In a high-frequency power output circuit, the base current required to charge the collector capacitance may run to several amperes, so that a thick contact is desirable on the base fingers as well.

Metal evaporation masks have been successfully made for the continuous-emitter structure (see Fig. 1 of the first quarterly report). Further masks are in process for the new separated emitter structure mentioned in section 4.3.7, where each emitter finger is connected to the backbone through a metal resistive layer. Two masks are required for this structure, one for the aluminum and one for the metal resistor. The first samples were produced with the latter mask only, the old KPR process described in the previous report being used to obtain the aluminum pattern. The aluminum thickness obtainable in this way is less than 0.5 μ owing to the inability of the KPR to withstand long etching times.

There has been difficulty in obtaining consistently good contacts with the thicker aluminum. Layers of thickness 1μ or greater tend to alloy deeply enough to destroy the emitter-base junction unless the temperature is very carefully controlled. A slightly lower temperature results in high contact resistance. A thin (0.3μ) layer tends to exhibit either high sheet resistance or high contact resistance.

There are two means being considered to overcome the above difficulty. A two-step process, where a thin Al layer is evaporated, alloyed, and a further Al layer of much greater thickness is subsequently evaporated, is being investigated. The oxide film forming on the first Al during alloying sometimes prevents good contact between the layers.

The other general means of contacting involves another metal in addition to the Al which would still be used to make ohmic connection to the silicon. A layer of Ag on top of the aluminum can provide the required conductivity with only one-half the thickness; however this will probably have to be applied in a two-step process. A further technique which has shown promise is to evaporate a thin layer (0.1μ) of Pd immediately following the Al evaporation in the same bell jar. This layer of Pd does not interact during alloying and protects the Al surface, so that an additional Al layer makes good contact.

4.3 Thermal Instability

4.3.1 Introduction

An important limitation on the power handling capability of thin, large area transistors arises from a lateral thermal instability which occurs at a certain critical internal temperature rise. Some aspects of this instability have previously been investigated at Shockley Laboratory,* where it was shown that hot spots occur as a result of the instability and probably lead to the phenomenon known as "secondary breakdown". The critical temperature rise is generally much lower than that which could be used on the basis of thermally generated currents and reliability considerations.

For example, on the transistors reported here, thermal instability and resultant second breakdown typically occurs at a power dissipation of 40 watts (at I_e = 1 amp) corresponding to an internal temperature rise of about 60°C. At lower current and higher voltage, the maximum power becomes less. However, it should be possible to operate these transistors at internal temperature rises of at least 150°C (for 50°C case temperature) without junction deterioration. It is evident that thermal instability seriously limits the power output capability of the device, and means of controlling this instability would result in significant improvement of device performance.

A simple physical picture of lateral thermal instability is given by the following. Consider a transistor with uniform emitter-base voltage and constant external emitter current. A reverse bias is applied to the collector junction so that the transistor is dissipating power, and

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* This work was carried out in part on Contract AF 30(602)-2556 with Rome Air Development Center

consequently the active region of the transistor rises to a higher temperature than the heat sink. Now suppose that the current density is not uniform, but fluctuates to a larger value in some localized part of the structure. A local temperature rise will then occur. The temperature coefficient of emitter current at constant forward bias is about 10% per °C. Thus the local temperature rise will produce a further increase in local current. If this further increase is larger than that which originally caused the temperature rise, an unstable situation exists and current can build up in one portion of the device and decrease in the remainder while the external current remains constant. A hot spot forms whose size is limited by resistive drops in the various layers of the transistor, and thermally generated current into the base layer from this hot spot may cause a local thermal runaway which is believed to be the condition termed "second breakdown".

Further theoretical investigation shows that several modes of instability can exist, but the mode with the most rapid buildup and whose critical temperature rise is lowest corresponds to the situation where one-half of the transistor is heating up and stealing current from the other half. Accordingly, when discussing the onset of instability, it is sufficient to consider this mode. The discussion below is carried out in terms of two parallel transistors, representing two halves of a single transistor. A key parameter known as the stability index is introduced. Means of improving thermal stability by effectively reducing the temperature coefficient of current, and two experimental approaches to achieving these results are described.

4.3.2 The Stability Index s for a Transistor

In order to introduce the influence of heating upon thermal instability we consider first the case of a transistor taken to be at a single temperature. We shall consider small deviations in current, voltage and

temperature from a set of initial values (see Fig. 2). . The symbols used are as follows:

$$V_1 = V_0 + v \tag{1a}$$

$$I_1 = I_0 + i \tag{1b}$$

$$U_1 = U_0 + u \tag{1c}$$

where V_0, I_0, and U_0 represent reference (usually steady state) values of voltage current and temperature, with temperature defined in equivalent voltage as

$$U = kT/q \tag{2}$$

where k is Boltzmann's constant, T temperature on the Kelvin scale, and q the electronic charge. The small letter symbols represent disturbances in the linear range of the phenomena investigated, and the quantities with subscript 1 represent the changed values.

Two functional relationships exist among the quantities considered:

$$I_1 = I_0 + i = F(U_1) = I_0 + I_0 au \tag{3}$$

$$dE_T(U_1)/dt = K\dot{u} = V_1 I_1 - H(U_1)$$

$$= V_0 i + I_0 v - hu \tag{4}$$

The first equation states that the current is a function of temperature (the collector current is supposed to be substantially independent of collector voltage); in the linear range of small disturbances its change is represented by a conductance g and a temperature coefficient a, so that

$$i = I_0 au \tag{5}$$

where $a = d(\log I)/dU \simeq i/I_o u$.

The second equation is the law of conservation of energy, which states that the rate of storage of heat energy E_T (which is the heat capacity K times rate of temperature rise $\dot{u}$) is equal to the net power $V_1 I_1$ minus $H(U_1)$ the rate of heat conduction to a heat sink at temperature $T_s = qU_s/k$. At the steady state condition, these powers $H(U_0)$ and $V_0 I_0$ exactly balance so that Eq. (4) involves only disturbances from equilibrium:

$$K\dot{u} = V_0 i + I_0 v - hu \tag{6}$$

where in the linear range

$$hu = H(U_1) - H(U_0) = udH/dU \tag{7}$$

As will be shown below, the existence of a negative real part for the impedance v/i depends upon a value greater than unity for a stability index s, defined as

$$s \equiv a V_0 I_0/h = (U_0 - U_s) a \tag{8}$$

To a first approximation $V_0 I_0/h$ is the rise in temperature in U-type units above the heat sink and is accurately this rise if heat flow is linear in temperature gradient so that

$$H(U) = (U - U_s)h \tag{9}$$

If the current depends exponentially upon temperature rises, then $s = 1$ corresponds to a current increase at fixed voltage by a factor of $e = \exp(1)$, the base of the natural logarithms.

It should be noted that a/h is a quantity independent of the temperature scale. It has the dimensions of Watt^{-1}. Thus, although the U in volts is algebraically more convenient to use in equations than is T in °K, the quantity a/h may equally well be calculated in terms of a_T, the temperature coefficient in (°K)$^{-1}$ of current increase at constant voltage, and of h_T, heat conductance in watts per °K. The relationship is

$$a_T/h_T = (a\ k/q)\,/\,(h\ k/q) = a/h \tag{10}$$

It is frequently more convenient to calculate s in terms of the a_T and h_T units:

$$s = a_T\ V_0\ I_0\ /h_T = (T_0 - T_s)\ a_T \tag{11}$$

where T_0 and T_s correspond to U_0 and U_s.

In order to understand why the stability index s is a critically important quantity, we consider first the case of zero frequency. Fig. 3 shows a V-I plot of equations (3) and (4) for two temperatures U_0 and U_1. The steady state condition for temperature U_0 is represented by the V_0, I_0 pair that simultaneously satisfies the two equations. Similarly, V_1 and I_1 satisfy the two equations for the higher temperature $U_1 = U_0 + u$. For the case shown, both v and i are positive and the transistor exhibits a positive low frequency conductance i/v.

The power inputs required for the two temperatures U_0 and U_1 are represented by two hyperbolae, each with constant input power VI, as shown in Fig. 3. For the case represented, it is seen that the point at the end of the dashed arrow at constant $V = V_0$ does not lead to the necessary power to produce a temperature rise u. It is evident that to reach $V_1 I_1$ an increase in V as well as in I is necessary.

If, however, the $h(U_1 - U_s)$ curve were much closer to the $h(U_0 - U_s)$ curve (a situation which would arise for high thermal resistance so that only a small increase in power produces a large temperature rise), then the arrow at constant V would lead to too much power and the $V_1 I_1$ point would correspond to an increase in I and a decrease in V, and a negative differential steady-state conductance.

That the dividing condition between positive and negative conductance corresponds to $s = 1$ may be seen by noting that in order for the increase in power due to the current increase I_0 au to be sufficient to sustain the increased temperature without any change in V, the relationship

$$V_0 I_0 au = hu \tag{12}$$

must hold so that

$$s \equiv a V_0 I_0 / h = 1 \tag{13}$$

This condition that $s = 1$ is a simple example of "self-balance"; when self-balance occurs, a disturbance in temperature produces at constant voltage exactly the change in power needed to compensate for the change in heat flow.

For large temperature rises there may be failure of the linear approximations leading to $s = 1$ for the stability condition. A more general condition can readily be derived from the self-balance condition. If it is assumed that a fluctuation produces an increase u above the steady state value U_0, then if the additional heat generated electrically at constant voltage exceeds the additional heat flow due to increased temperature, the fluctuation will grow and instability will occur. Self-balance is the dividing condition between stability and instability and can be expressed

conveniently in terms of fractional changes in electrical and thermal powers, since the steady state powers I_0V_0 and $H(U_0)$ are equal. Fractional changes are, of course, equal to changes in logarithms. Furthermore, since V_0 is constant the change in log V_0I_0 equals the change in I_0. Hence, taking rates of change instead of changes themselves, we obtain

$$\partial \log I/\partial \log U \leq \partial \log H(U)/\partial \log U \tag{14}$$

where the derivatives are evaluated at U_0, I_0 and V_0. When $H(U_0)$ is proportional to the rise above the heat sink temperature U_s, this condition reduces to

$$a U_0 \leq U_0/(U_0 - U_s) \tag{15}$$

or

$$(U_0 - U_s)\, a \leq 1 \tag{16}$$

in keeping with equations (8) and (9).

4.3.3 The Temperature Coefficient of a Transistor

This study is chiefly concerned with thermal instability caused by the increases in current through the base layer of a junction transistor produced by increase of temperature. This effect causes the transistor to simulate a thermistor having a high positive temperature coefficient of conductance.

Fig. 2 illustrates the configuration studied in this section. An npn transistor is represented. It is represented essentially as a two-terminal device carrying a current I with an applied voltage V. Internal to the device there is a base voltage supply V_b which maintains the base voltage. For most cases of practical interest the power dissipation due to the base current and the base emitter voltage is negligible. In special

cases this power dissipation may have to be considered, but we shall in general neglect it here.

In analyzing the behavior of the transistor in the circuit of Fig. 2, we shall consider how the collector current depends upon temperature and base voltage and also how the base voltage depends upon temperature for constant collector current. We shall neglect recombination in the base layer in this treatment, so that the current of importance is the collector current, denoted by I. As a starting point we shall assume that a uniform forward bias V_b exists over the area A of the emitter-base junction. If the total charge of uncompensated acceptors per square centimeter of the base layer is Q, and the diffusion constant for electrons is D_n, then this current may be expressed as

$$I = (A\, q^2\, n_i^2\, D_n/Q) \exp (V_b/U) \tag{17}$$

where q is the electronic charge and n_i is the electron or hole density in intrinsic material. U is the temperature expressed in electron volts:

$$U = kT/q \quad ; \quad T/U = q/k = 11,600\ ^\circ K/\text{volt} \tag{18}$$

where k is Boltzmann's constant. In this expression n_i and D_n are both dependent upon temperature. Over a range of temperature sufficiently broad to cover the studies undertaken here, the dependences of n_i^2 and D_n upon temperature can be expressed as follows:

$$\ell n\ D_n = \ell n\ (kT\mu_n/q) = (1 + n_{\mu n})\ \ell n T + \text{const} \tag{19}$$

$$\ell n\ n_i^2 = n_{pn}\ \ell n\ T - (V_g/U) + \text{const} \tag{20}$$

Combining these expressions with expression (17) leads to

$$\ell n\, I = n_T\, \ell n\, U + (V_b - V_g)/U + \text{const} \tag{21}$$

where the power n_T is given by

$$n_T = 1 + n_{\mu n} + n_{pn} \tag{22}$$

The desired derivatives of current in respect to voltage and temperature are readily obtained by Eq. (21). It is mathematically convenient to express these in terms of logarithmic derivatives which can be readily altered to give derivatives in respect to the variables involved. The total differential of Eq. (21) is

$$d\, \ell n\, I = [n_T + (V_g - V_b)/U]\, d\, \ell n\, U + d\, V_b/U \tag{23}$$

The partial derivative of $\ell n\, I$ in respect to $\ell n\, U$ at constant V_b is readily found to be

$$a_o \equiv \left(\frac{\partial\, \ell n\, I}{\partial\, \ell n\, U}\right)_{V_b} = (V_g - V_b)/U + n_T \tag{24}$$

This quantity, which has no dimensions, would be the slope of the current versus temperature line on a sheet of log-log graph paper. It is related to the coefficient a, discussed in the previous section, as follows

$$a \equiv \left(\frac{\partial\, \ell n\, I}{\partial\, U}\right)_{V_b} = \left(\frac{\partial\, \ell n\, I}{\partial\, \ell n\, U}\right)_{V_b} \div U \equiv a_o/U \tag{25}$$

Since $\ell n\, U$ and $\ell n\, T$ differ by a constant, it may readily be seen that the coefficient of current change in respect to temperature in degrees Kelvin is given by

$$a_T = \left(\frac{\partial\, \ell n\, I}{\partial\, T}\right)_{V_b} = a_o/T \tag{26}$$

As an example of the order of magnitude of the quantities involved, we shall consider a particular case of a transistor having a charge of 10^{-6} coulombs per square centimeter of the base layer at room temperature and under conditions in which the current density is 1 A/cm^2. For silicon under these conditions the quantities needed for evaluating the temperature coefficient are as follows:

$$q = 1.6 \times 10^{-19} \text{ coul} \tag{27a}$$

$$Q = 10^{-6} \text{ coul/cm}^2 \tag{27b}$$

$$n_i^2 = 2.2 \times 10^{20} \text{ cm}^{-6} \text{ at } 293\ ^\circ\text{K} \tag{27c}$$

$$n_{pn} = 3 \tag{27d}$$

$$V_g = 1.21 \text{ electron volts} \tag{27e}$$

$$D_n = 35 \text{ cm}^2/\text{sec} \tag{27f}$$

$$n_{\mu n} = 2.5 \tag{27g}$$

$$n_T = 1 - 2.5 + 3 = 1.5 \tag{27h}$$

$$I/A = 1 \text{ amp/cm}^2 \tag{27i}$$

$$U = kT/q = 293^\circ/11,600 = .025 \text{ volts} \tag{27j}$$

From these values the remaining single unknown V_b of Eq. (17) can be found:

$$V_b = U \ln QI/A\, q^2 n_i^2 D_n$$

$$= 0.025 \ln 10^{-6}/(1.6 \times 10^{-19})^2 \times 2.2 \times 10^{20} \times 35$$

$$= 0.025 \ln 0.52 \times 10^9 = 0.50 \text{ volts} \tag{28}$$

Substituting these values in Eq. (24) leads to

$$a_o = [\,(1.21 - 0.5)/0.025\,] + 1.5$$

$$= 28.4 + 1.5 \cong 30 \qquad (29)$$

from which it is seen that in the operating range the current in effect depends upon a very high power of the temperature. Expressed as a temperature coefficient on the Kelvin scale, we obtain

$$a_T = a_o/T = 0.1\ °K^{-1} \qquad (30)$$

which signifies a change of approximately 10% in current for each degree increase in temperature on the Kelvin scale, or a factor of e increase in current for each 10°K.

The condition for which the arrangement of Fig. 2 will exhibit a negative resistance can now be expressed in terms of quantities familiar in connection with transistor design. A typical value for thermal resistance of a power transistor is 2°C per watt, leading to a value for the thermal conductance of $h_T = 0.5$ watt/°K. This leads to a relatively simple expression for the stability index s of Eq. (11): $s = a_T VI/h_T \cong VI/5$. For this particular example the transistor will exhibit a negative differential resistance on its V-I characteristic if the power exceeds 5 watts. Most practical transistors have sufficient internal ohmic resistance to modify this result, in a manner to be indicated below.

In analytic studies of thermal effects over large factors of change in current, it is convenient to use the approximation

$$I(U) = I_s \exp[\,(U - U_s)\,a\,] \qquad (31)$$

where I_s is the current which would flow if the transistor were at the temperature U_s of the heat sink and U is the actual temperature, it being assumed that the emitter-base voltage is constant. This approximation involves the error of assuming that

$$\ell n\, I - \ell n\, I_s = (U - U_s)a \tag{32}$$

where

$$a = a_o\,(U_s)/U_s \tag{33}$$

This error is equivalent to using only the first term of a Taylor's expansion of $\ell n\, I$ in Eq. (21). The correct Taylor's expansion to two terms is

$$\begin{aligned} \ell n\, I - \ell n\, I_s &= \{ (n/U_s) + [(V_g - V_b)/U_s^2] \} (U - U_s) \\ &\quad - \{ (n/U_s^2) + 2 [(V_g - V_b)/ U_s^3] \} (U - U_s)^2/2 \\ &= a(U - U_s) - [a - (n_T / 2 U_s)] (U - U_s)^2 / U_s \\ &= a(U - U_s) \{ 1 - [1 - (n_T / 2aU_s)] (U - U_s)/U_s \} \end{aligned} \tag{34}$$

For many cases of interest the correction term is practically negligible, as can be seen as follows: a $U_s = a_0$, which is approximately 30. Hence the $n_T / 2aU_s$ term is small compared to unity. For cases of interest $a(U - U_s)$ is approximately unity, so that

$$\begin{aligned} 1 \doteq a(U - U_s) &= a\, U_s (U - U_s)/U_s \\ &= a_0 (U - U_s)/U_s \end{aligned} \tag{35}$$

Hence $(U - U_s)/U_s \doteq 1/a_0$. Thus the correction to the first term of the Taylor's expansion is only a few percent, and it is satisfactory to use (31).

For large variations in temperature it is sometimes necessary to take into account changes in a_0. These are usually small, provided the current density is kept constant. This conclusion may be reached by writing a_0 in the form

$$a_0 = [(V_g - V_b) / U] + n_T \tag{36}$$

where from equation (17) we obtain

$$(V_g - V_b) / U = -\log I\Omega/A\, q^2 D_n n_i^2 \exp (V_g / U)$$

$$= -\log I + n_T \log U + \text{const.} \tag{37}$$

In this expression V_b is the forward voltage across the emitter junction. For the case where $(V_g - V_b) / U$ is the order of 30, changes of a factor of two in absolute temperature will change $(V_g - V_b) / U$ by less than 10% from the $n_T \log U$ term.

4.3.4 Instability of Two Parallel Transistors and of Large Area Transistors

If two transistors are connected in parallel and sufficient current is passed through them to produce a negative resistance condition, then a phenomenon known as "current-hogging" will occur. This condition corresponds to an instability building up, in which one transistor carries more current than the other and consequently becomes warmer and drops its resistance. This inequality then tends to build up until finally essentially all of the current is going through one of the transistors and the other one is relatively cool and carries little current.

The instability condition depends not only upon the characteristics of the individual transistors but also upon the ability of heat exchange to

take place between the two of them. This situation is represented schematically in Fig. 4(a),where the boxes represent transistors connected as in Fig. 2 with the same base voltage. In this figure the thermal conductances of each transistor to a heat sink are represented by the heat conductance h. On the figure, heat conductances are represented by wavy lines and electrical conductances by straight lines. There is also assumed to be a mutual heat conductance m between the two transistors. Evidently, if the two transistors were actually connected mechanically into such intimate contact that there could be no temperature difference between them, then it would be impossible for one of them to become heated in respect to the other and carry substantially all of the current.

The problem of this section is to derive the analytical conditions determining the stability of the pair of parallel transistors. This stability problem is very similar to the problem of hot spot generation in a power transistor, in which one portion of the power transistor takes over all of the current and becomes warm, leaving the rest of the transistor relatively cool.

We assume that for each transistor by itself a point on the V-I characteristic corresponds to values V_0 and I_0. We further assume that the external current is kept constant at $2\,I_0$. The disturbed condition for the parallel circuit is represented on the figure, with current i_1 representing the disturbance in current through each of the two transistors, positive in one and negative in the other. The corresponding temperature disturbance is u.

The increment in heat flow away from the transistor on the right is evidently hu (to the heat sink) plus mu - (-mu) = 2 mu (to the transistor on the left). Hence the disturbance in temperature u results in

an increased heat flow of (h + 2 m) u, so that the effective thermal conductance is h + 2 m, as shown in Fig. 4(b). This corresponds to the fact that the unstable behavior involves one transistor heating up and the other one cooling down by an equal amount, so that the conductance of heat through the mutual conductance m is twice as great as if one side were held at a fixed temperature.

It should particularly be noted that the disturbance under consideration occurs independently of the impedance of the external power source so that no changes in this source can influence the instability until the disturbance exceeds the amplitude where the linear approximations are valid.

The stability condition corresponding to the equivalent circuit of Fig. 4(b) is evidently

$$s_2 = a V_0 I_0 / (h + 2m) \tag{38}$$

in a form analogous to that of Eq. (8) for a single uniform transistor. Although this thermal instability condition is the important one for our consideration, it is worthwhile to point out that there is another instability which depends on the impedance of the external power source. This is the situation where current builds up in an identical manner in each transistor, and the pair act like a single transistor. The stability index in this case is evidently $s = a V_0 I_0 / h$ as given by Eq. (8). If the external current is controlled as in Fig. 4, this instability does not arise; however if the pair were supplied from a voltage source, current would begin to build up in both when $s = 1$.

The condition $s_2 = 1$ is a second example of self-balance. (Self-balance was discussed in connection with Eq. (13) and is closely related

to the problem of instability of the distributed structure where one half of the transistor steals current from the other half.) For the parallel transistor case, when $s_2 = 1$, a slight increase of current in transistor 1 and equal decrease in transistor 2 results in a disturbance of power which exactly balances the disturbances in heat flow -- again a self-balance situation. So far as the thermal properties are concerned, the stability condition does not involve the heat capacitances but only the heat conductances. This is because for $s_2 = 1$ neither build-up nor decay occurs, so that no temperatures change; consequently, no power flow to heat capacitances is involved. An increase in general power level, making $s_2 > 1$, will destroy the self-balance and will result in more electrical power change than needed for the changed thermal energy flows. The rate of build-up will then depend on the heat capacitances.

The stability condition $s_2 = 1$ is most severe for a large area power transistor where the distance from the collector junction to an effective heat sink is much less than the lateral dimensions of the device. In such a case, the lateral thermal conductance m (see Fig. 4) is evidently much less than the thermal conductance h to the heat sink, and the condition $s_2 = 1$ occurs at almost the same power level as that required for the transistor as a whole to be unstable when connected to a voltage source ($s = 1$). However, it is again emphasized that the instability occurring when $s_2 = 1$ is independent of the power source impedance.

It should be noted that our discussion has dealt analytically only with the small signal disturbance. It is difficult to extend the treatment analytically to large signals, but graphical methods can be used to visualize the results which will occur. The important criterion is generally the one which governs the initiation of the instability. After this, in general, it will proceed to some physically recognizable limit, where

spreading resistance controls the ultimate size of the hot spot. In the case of a power transistor, other adverse limitations may occur, such as concentration of the current to such a degree that the device is destroyed by local heating.

4.3.5 The Resistive Emitter Layer

A material improvement in the power handling capacity of a power transistor or similar device with thermistor-like behavior can be achieved by placing a resistive layer between the metal emitter contact and the emitter-base junction. We shall refer to such a layer as a "resistive emitter layer."

We consider a transistor with a series emitter resistor, as shown in Fig. 5. This is a lumped constant version of the resistive emitter layer case. The lumped constant version shows that very substantial reductions of the temperature coefficient of current can be produced. The consequence is that much higher power levels may be achieved without negative resistance occurring.

In keeping with Eq. 17, with V_b replaced by $V_b - RI_e$, if the transistor operates uniformly over its emitter area A and the charge of uncompensated acceptors in the base layer is Q per square centimeter, and the recombination in the space charge layer and in the emitter is neglected, then the total emitter current through the transistor is given by:

$$I_e = (A\, q^2\, n_i^2\, D_n/Q) \exp (V_b - RI_e)/U \qquad (39)$$

If recombination modifies alpha, the emitter current can still be taken for most purposes to have the same dependence on voltage as Eq. (39). In this equation both the intrinsic carrier density n_i and the diffusion

constant for the electrons diffusing through the base D_n depend upon temperature. As discussed in connection with Eqs. (19) and (20), this may be expressed as follows:

$$d \ln (n_i^2 D_n) / d \ln U = n_T + (V_g / U) \tag{40}$$

The temperature-dependent coefficient in the intrinsic density term varies as the cube of the temperature. The diffusion constant depends on temperature to one higher power of T and hence of U than does the mobility, which depends on temperature to the minus 2.5 power for electrons in silicon. Hence n_T has the value

$$n_T = 3 + 1 - n_{\mu n} = 1.5 \tag{41}$$

The partial derivatives of I in respect to temperature and to applied base voltage may be readily calculated from Eq. (39). In Eq. (39) the term $R I_e$ is the emitter voltage which we shall denote as V_{er}, so that $V_b - R I_e$ is the forward emitter-base voltage. Taking the total differential of Eq. (39) we readily obtain

$$\begin{aligned} d \ln I_e = & \{ n_r + [(V_g + R I_e - V_b) / U] \\ & - (R I_e / U) \, d \ln R / d \ln U \} \, d \ln U \\ & - (R I_e / U) \, d \ln I_e + d V_b / U \end{aligned} \tag{42}$$

If alpha is independent of current, $d \ln I_c$ will equal $d \ln I_e$. In keeping with the notation of Eq. (24), we introduce the symbol a_0 which is the value of the logarithmic derivative of current in respect to the logarithm of temperature when the base-emitter voltage $V_b - V_e$ is independent of temperature; a situation which occurs if R vanishes. The quantity a_0 is chiefly determined by $(V_g + V_{er} - V_b) / U$. As discussed in connection

with Eq. (37), this term, which is $(V_g + R I_e - V_b) / U$ in Eq. (42), is determined for a given transistor structure chiefly by the current density and is only slightly affected by temperature. Note that a_0 decreases by a factor of 2.3 for every ten times increase in current density. The value of a_0

$$a_0 = n_T + (V_g + R I_e - V_b) / U \tag{43}$$

thus represents the derivative of log I_e in respect to log U at the same current density I_e/A as in Eq. (42) but for a base emitter-voltage independent of temperature as if no emitter resistor were present.

When the resistance R is present so that $V_{er} = R I_e$ does depend on U, the actual partial derivative denoted by a_{0r} of log I_e in respect to log U is obtained from Eq. (42) and has the value

$$a_{0r} = \left(\frac{\partial \ln I_e}{\partial \ln U}\right) = a_0 \left[1 - (n_r/a_0) (d \ln R / d \ln U \right] / (1 + n_r) \tag{44}$$

where n_r is defined as the number of thermal units of voltage required to produce the drop across R:

$$n_r \equiv R I_e / U = V_{er} / U \tag{45}$$

The reduction of a_0 to a_{0r} by the action of R may be represented by a factor f_r where

$$f_r = a_{0r}/a_0 = [1 - (n_r/a_0) (d \ln R/d \ln U)] / (1 + n_r) \tag{46}$$

It is seen that a_{0r} may be reduced by a substantial amount if the drop across the series resistance is large compared to thermal voltage. In general, the correction term in the numerator will be small since the

coefficient a_0 is the order of 30, and the logarithmic derivative of resistance will be of the order of unity. Only if the resistance decreases with increasing temperature will the numerator of Eq. (44) contribute to an increase of a_{0r}.

The occurrence of negative resistance for this configuration is based on the stability index s_r, which is decreased by the presence of the resistance R from the value without it. This stability index is defined as usual as the coefficient of current increase per unit temperature rise times the temperature rise. This latter is represented by the power input which is essentially the voltage V times the collector current I_c, divided by the thermal conductance of the device. The symbol h represents the thermal conductance when temperature is measured in electron volt units in keeping with U as in Eq. (2). In accordance with this definition, the stability index can be written in the following forms:

$$s_r = (a_{0r}/U)(V I_c/h) = (a_{0r}/a_0)\, a_0\, V I_e/h U$$

$$= (a_{0r}/a_0)\, s = f_r\, s \qquad (47)$$

where s is defined in keeping with Eq. (8) except that the subscript "0" has been omitted. For transistors with values of alpha near unity I_c, the collector current, can be replaced by I_e. In some extreme cases the power generated in R must also be included. The symbol s can also be written in the form

$$s = (T - T_s)\, a_T \qquad (48)$$

where a_T is the coefficient of increase of current with temperature measured in degrees Kelvin and $T - T_s$ is the temperature rise in the transistor above the ambient.

The stability index with the resistance present is seen to be reduced by a factor corresponding to the fraction f_r in Eq. (46). If the drop across the series resistance is one or two tenths of a volt, then this fraction is the order of one-fourth or one-eighth, so that a very substantial reduction of stability index for a given power level can be achieved by relatively small voltage drops or, conversely, a given stability index can be achieved at four to eight times the power level.

For cases of large temperature rises, which become possible for large values of n_r, it is necessary to note that the power H(U) carried away as heat to the heat sink does not vary proportionately with the difference between the steady state temperature U and the heat sink temperature U_s. The application of potential theory and the laws of heat flow can be applied to show that if the thermal conductivity c is a function c(U) of the temperature, then

$$H(U) = h(U_s) \int_{U_s}^{U} [\, c(U) / c(U_s) \,]\, d\, U_s \qquad (49)$$

where $h(U_s)$ is the thermal conductance of Eq. (7) for small deviations from the temperature U_s. For $U - U_s$ so small that $c(U)/c(U_s)$ is nearly unity, this reduces to the linear result $h(U_s)\,(U - U_s)$.

For silicon from T = 300°K to about 700°K, $c_T(T)$ can be well approximated by [5]

$$c_T(T) = 1.1\ (300/T)\ \text{watts/cm°K} \qquad (50)$$

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5. R. G. Morris and Jerome G. Hust, Phys. Rev. 124, 1426 (1961)

For this behavior, Eq. (49) reduces to

$$H(U) = h(U_s)\, U_s \log (U/U_s) \tag{51}$$

This equation can be used in the self-balance condition discussed following Eq. (13) to determine the stability limit. Equations equivalent to (51) can be derived for more exact expressions for $c_T(T)$.

The self-balance condition corresponding to $s_r = 1$ is given by Eq. (14):

$$\partial \ln I / \partial \ln U < \partial \ln H / \partial \ln U \tag{52}$$

at constant voltage. For a transistor with an alpha nearly independent of temperature, collector and emitter current have the same derivatives of their logarithms and inequality (52) reduces to

$$a_{0r} = a_0 f_r < 1/\log (U/U_s) \tag{53}$$

In this equation a_{0r}, a_0 and f_r all are evaluated at U. For $U - U_s$ small compared to U_s, this stability condition reduces to Eq. (48). For large temperature rises, such that f_r must be much less than unity to satisfy (53)the approximation

$$f_r = 1/n_r \tag{54}$$

can be employed and the voltage drop across R then becomes

$$V_{er} = n_r U = U/f_r > a_0 U_s (U/U_s) \log (U/U_s) \tag{55}$$

For the silicon transistor example of Eq. (27), the required values

are as follows: $T_s = 300°K$ and $U_s = 0.025$ volts and $a_0 = 30$. (a_0 for a given current density is nearly independent of U as discussed following Eq. (35). This leads to

$$V_{er} = n_r U > 0.75\,(U/U_s)\ln(U/U_s)\ \text{volt}$$

$$= 0.75\,(T/300°K)\ln(T/300°K)\ \text{volt} \qquad (56)$$

For several temperatures, the voltage drops $n_r U$ required for stabilization are shown in Table I.

Table I

Emitter voltage drops required for thermal stabilization

$T - T_s$ °C	50	100	200	300
T °C	77	127	227	327
T °K	350	400	500	600
$n_r U$ volts	0.13	0.29	0.64	1.05

Without the use of the resistor, negative resistance and lateral instability would occur for $T - T_s = 10°C$ as discussed following Eq. (30). The above table shows, for example, that an emitter resistor producing a 0.64 volt drop at the operating current will stabilize the transistor up to a 200°C internal temperature rise.

The discussion to this point has considered the reduction in the temperature coefficient a_0 of a uniform transistor by means of an emitter resistor. However, a large area transistor cannot be internally stabilized by means of a single external emitter resistor, since an internal instability of the sort discussed in 4.3.4 above does not require any change

in external emitter current and the resistor is thus ineffective. Evidently, each half of the transistor must be provided with an independent resistor. Now, however, one half may become unstable within itself and further subdivision be required. It is clear that the best form that the emitter resistor can take is that of a distributed layer between the emitter proper and the emitter metal contact, as shown in Fig. 6. Consider such a resistive layer having a resistance of R_r ohms for a region of area one cm^2. If the layer consists of material of resistivity ρ_r and thickness w, then

$$R_r = \rho_r w \text{ ohm - } cm^2 \tag{57}$$

and the lateral resistance will be

$$R_{sr} = \rho_r / w = R_r / w^2 \text{ ohms/square} \tag{58}$$

The quantity R_r is important in the mathematical formulation of stability; R_{sr} is of interest in connection with measurements of deposited layers for purposes of control.

If the emitter current density J(x) is a function of lateral distance x across the device, then n_r of Eq. (45) is a function of x also:

$$n_r(x) = J(x) R_r / U \tag{59}$$

It is evident that this quantity for the case of varying emitter current density will make the greatest contribution to stability in the location where it is most needed, namely where the current and power densities and the temperature rises are highest.

4.3.6 Epitaxial Resistive Layers

4.3.6.1 Choice of Material

It appears particularly favorable to utilize epitaxial techniques for the purpose of producing a distributed resistance like that of Fig. 6. There are several reasons for this choice. A layer of epitaxial silicon has the same coefficient of thermal expansion as the transistor body itself. The desirable range of resistivity can be achieved more easily than with metals or insulators. A desirable positive temperature coefficient of resistance should also be attainable with a silicon layer.

Initial estimates for the design of a resistive layer show that the layer thickness should be approximately 1 micron and the layer resistivity of the order of 10 ohm-cm. From Eq. (57), R_r is 10^{-3} ohm-cm^2 for this layer. From Eq. (59), this layer provides a voltage drop $n_r U$ of 0.2 volts at a current density of 200 a/cm^2. It should be easy, in principle, to meet these specifications.

It was therefore decided to pursue this method further. The technology of epitaxial deposition is reasonably well under control and available.

4.3.6.2 Oxide Masking

A resistive layer should only be deposited directly above the emitter. The base or collector regions should not be covered. This requires a suitable masking technique for the deposition. Silicon dioxide (SiO_2) can be utilized for this purpose. All portions of the transistor surface, except the emitter area, are masked by such oxide, which has been grown during the preparation of the emitter.

The emitter area can be opened by etching with ammonium fluoride.

The epitaxial layer can be restricted to this open emitter area for short deposition time. However, there is very often a spurious overgrowth of polycrystalline silicon over the adjoining oxide layers. Such overgrowth is undesirable since it presents considerable difficulties for the further processing of the transistor structure.

The overgrowth is very non-uniform. Oxide areas close to the opened emitter are less affected than areas farther removed. The total amount of polycrystalline overgrowth was substantially reduced by providing more area of unprotected silicon. For this purpose the oxide was removed from the regions between devices. These regions are unused and normally etched away during dicing. Without oxide, however, they serve as additional nucleation centers for epitaxy. We believe that thus one can reduce the chance for the supersaturation of silicon-compounds or radicals, which seems to be necessary for growth of Si on SiO_2.

If the growing time is substantially longer than approximately five minutes, the polycrystalline growth will take place regardless of the structure. This fact seriously limits the growing time and means that the thickness of the epitaxial deposition is limited.

A serious problem arises from the heating of the slice which is necessary for epitaxy. This treatment causes diffusion, thus changing the device structure. Therefore, the epitaxial deposition should take place at low temperatures for short times and with high deposition rate. The preceding diffusions must be adjusted to the epitaxy heat treatment.

Before the experiments were carried out, it was anticipated that an etching of the oxide layer during the deposition would take place and

thus constitute another limitation. In all of our experiments, this was not observed and does not present a problem.

4. 3. 6. 3 Deposition Schedule

The deposition of the silicon was done by means of a conventional thermal decomposition technique. $SiCl_4$ is reduced in a hydrogen atmosphere at approximately 1150°C. A standard apparatus with rf heating is used. The growing procedure is slightly modified. The temperature is lower than is normally used. The deposition time is very short (less than 5 minutes). Heating of the slice before and after deposition is reduced to a minimum.

It was attempted to produce layers with as high a resistivity as possible. This can only be achieved by means of compensation with a p-type doping agent such as BCl_3 since the underlying n^+ material contributes to the doping of the resistive layers. It was, however, possible to obtain layers of approximately 1 micron thickness which had a resistivity of the order of 1 ohm centimeter.

Figure 7 shows part of a transistor structure with an epitaxial resistive layer.

The crystalline perfection of the layer is of minor importance for the functioning as a distributed resistance. It was observed that there is a considerable density of stacking faults in most of the deposited silicon layers. This seems to be related to the contamination by the oxide.[6]

6. R. H. Finch et al, J. Appl. Phys., February 1963.

4.3.6.4 Contacts

It was decided to contact the resistive layer with an evaporated aluminum film. This contact is the same as that for the regular power transistor structure without a resistive layer. In order to compare power handling capacities, no changes of the contact are desirable.

Aluminum contacts to n-type materials require a minimum doping level in the silicon in order to avoid a rectifying contact. It was therefore necessary to deposit a heavily doped silicon layer on top of the lightly doped resistive layer. This was done either by a phosphorus diffusion or a subsequent short epitaxial deposition directly after the deposition of the resistive layer. Onto these structures aluminum was then evaporated and alloyed.

4.3.6.5 Evaluation

Before application of this technique to actual devices it was necessary to make several trial runs. These runs served as calibration experiments for thickness, resistivity, and temperature coefficient of resistivity of the deposited thin layers.

The thickness was measured either with an infrared spectrophotometer or by standard bevelling and staining techniques.

The resistivity was measured with a novel method which is described in detail in Appendix A. This method consists of potential probing on a fine scale (down to 2 microns distance between measuring points). It is possible to obtain both the sheet conductance (ohms/square) of the n^+ layer as well as the transverse conductance (ohm-cm^2) of the resistive n^- layer. These measurements were useful in calibrating the time,

temperature, and doping conditions during the epitaxial deposition. The results indicated that only with compensation was it possible to obtain thin, highly resistive layers.

The results in Appendix A were obtained on an early sample where growing time was not limited by overgrowth occurring on the oxide layer as discussed above. It has not been possible to duplicate these results on an actual transistor, where the R_r obtained has been 50 times less than that in Appendix A. It is desirable to have a resistive layer with a positive temperature coefficient of resistivity. Such a positive coefficient leads to a further stabilization of a current distribution. It was therefore necessary to check the temperature coefficient of the resistivity for these epitaxial silicon layers. These measurements were done with a modified four point probe method at temperatures between room temperature and approximately 250°C. The results indicated that only uncompensated silicon has the desirable positive temperature coefficient. Compensated epitaxial layers, on the other hand, have always shown negative temperature coefficients. This result seems unfavorable since it indicates that with the present state of the art it is very difficult to meet both requirements of a high resistivity and a positive temperature coefficient.

4.3.6.6 Results on Actual Power Transistors

Approximately ten transistors were produced with epitaxially-grown resistive emitter layers. The standard saturation voltage measurement was performed (I_c = 5 a, I_B = 0.5 a) to detect the presence of the extra emitter resistance. The results indicated that this extra resistance was less than about 0.03 ohms in all cases, corresponding to an R_r of the order of 2×10^{-4} ohm-cm^2. This is a factor of 5 smaller than the design value, and does not contribute any significant stabilization.

Hot spots were observed to develop (see Section 4.5.1) at about the same power level as on similar transistors without resistive layers.

The lower resistance than expected is connected with the diffusion and migration of impurities from the n^+ emitter during growth, and with the degree of control obtained in producing the subsequent n^+ layer needed for contact. Experiments involving the growth of thicker, more highly compensated layers are continuing.

4.3.7 Lumped Emitter Resistors

Difficulties in producing a distributed emitter resistance led to a scheme of introducing discrete resistors in series with each emitter finger of the interdigitated structure (see Fig. 1 of the First Quarterly Report). In this way, no one finger can develop a hot spot and take a large fraction of the total current. Since there are 32 fingers, the structure is quite finely divided.

In order for this scheme to work, the emitter diffusion must be made only in each finger region, and the emitter backbone which serves as a common bus bar, must be isolated from the transistor by an oxide layer. Fig. 8 shows one finger connected to the backbone by means of an evaporated metal resistor.

Each of these resistors should have a resistance of about 6 ohms for stabilization at a total current of 1 ampere, giving a voltage drop in each finger of $6 \times 1/32 \simeq 0.2$ volts (see Table I in Section 4.3.5). Since the metal resistor consists of nearly 2 squares in series, its sheet resistance R_s is required to be about 3 ohms/square. If its thickness is w, the resistivity needed is $\rho = w R_s$. It is considered undesirable to have a layer thickness of less than $0.03\ \mu = 3 \times 10^{-5}$ cm, so the minimum resistivity is about 10 μohm-cm.

In addition to the high resistivity of at least 10^{-5} ohm-cm, the metal should have a relatively low melting point and should be chemically inert. Some metals which have these properties are Ti, Zr, V, Nb, Cr and Pd. Experiments have shown that Pd and Cr are both desirable metals because of their relatively low melting points and high vapor pressures in addition to their chemical inertness. Ti, V, Nb and Zr were found to be unsuitable because of their low vapor pressures at temperatures attainable. Table II shows the resistivity, melting point, and temperature where the vapor pressure is 10^{-2} mm Hg.

Pd films of various thicknesses were evaporated onto glass substrates in order to determine evaporation conditions and film characteristics. The first method used was the evaporation of definite quantities of Pd powder from a heated Mo boat. This procedure was shown to be inadequate because a high enough temperature for evaporating the Pd rapidly and completely could not be attained. The second method used was the evaporation of thin Pd wires from a heated W rod. By this procedure we obtained the desired rapid, complete, and reproducible evaporation. Plots of the measured thickness vs length of wire evaporated, sheet resistance vs thickness, and sheet resistance vs temperature were drawn from experimental values. The temperature coefficient of sheet resistance is positive and is about 4.2×10^{-3} deg^{-1} in the range 20°-160°C.

Pd films were evaporated onto power transistors in the geometry of Fig. 3.7. Some of the resulting devices showed improved thermal stability characteristics. However, difficulties arising from the alloying of the Pd and the Al necessary for the emitter contact layer make it necessary to study this alloying process further.

It may be possible to avoid the alloying difficulties encountered by evaporating resistive layers of Cr instead of Pd. Experiments to

determine the suitability of Cr films have been started using Cr powder evaporated from a Ta boat.

Another possible way to avoid the problems encountered with Pd is to evaporate Nichrome resistive layers. Initial experiments have involved the evaporation of Nichrome wire.

Table II

Properties of metals for emitter resistors

Element	$\rho \times 10^6$ (Ω cm)	m.p. (°C)	T where v.p. = 10^{-2} mm Hg(°C)
Ti	43.5	1667	1737
Zr	41	1855	2397
V	19	1917	1847
Nb	13	2497	2657
Cr	15	1903	1397
Pd	10.9	1550	1462

4.4 Packaging

The double-ended stud mounted package described in the last report has been modified for better thermal and electrical performance. Fig. 9 shows an exploded view of the new package, and it should be noted that the vertical dimensions are exaggerated by about 30%.

A one-piece copper base (plus weld ring) has holes drilled to accept the beryllia insulator and standoff insulators to hold the lower end of the connectors. The W metallized beryllia disk providing electrical isolation of the device has been greatly reduced in size from the previous design. The present disk is 1/4" in diameter and 30 mils thick, and is soldered with Incusil to the copper base. The device is alloyed to a gold-plated Mo disk (1/4" diameter, 10 mils thick) as previously, and this disk mounted on the beryllia with Au-Ge solder as described in the previous report. The can has been reduced in height from about 11 mm to 8 mm and provided with spade lugs.

An estimated conservative value of thermal resistance of the package from the Mo disk surface to the copper stud is 0.5°C/watt, of which about 70% arises in the Mo disk. These figures take into account spreading from the effective heat generation area of the transistor.

Figure 10 is a view of the assembled package without the can, and Fig. 11 shows the complete package. Multiple gold wires are used to connect to the collector (Mo disk); these may be replaced with ribbon. Twin emitter leads are provided for minimum feedback due to emitter lead inductance in common-emitter circuits. If desired, twin base leads could be provided for common-base circuits.

The continued contributions of E. Brown are acknowledged.

4.5 Electrical and Thermal Evaluation

4.5.1 General

Approximately 107 good experimental devices were made during the quarter. Table III shows the various runs (exclusive of those made to test thermal stabilization techniques - see section 4.3) with typical parameters. All of these transistors were made on 15 Ω - cm n^- n^+ inverse epitaxy (see section 4.3 of the preceding report) whose n^- layer thickness varied from about 13 to 25 μ. Differences between the runs are chiefly those of diffusion schedules. Runs 8 to 12 employed the old geometry with 400 μ finger length, while all later runs were made with 560 μ finger length. Since suitable metal masks were not available at the time, these transistors all have an aluminum contact thickness of about 0.3 μ, which is considerably thinner than that required for best performance. The thin aluminum results in higher thermal resistance and lower β (h_{FE}) at high currents. In addition, it is likely to degrade seriously the high power r.f. performance. Various techniques for producing thicker metal contacts are being investigated.

It is to be noted that the current gain h_{FE} at 5 amperes collector current is considerably improved starting at run 14. One reason is the 40% greater active area introduced with this run; another is that some of the deeper diffused structures (indicated by the notation D) should have higher emitter efficiency than the shallow diffusions, since the emitter width is larger with respect to the base width.

The large collector-base capacitance C_{ob} appearing in a number of runs is a result of the relatively thin 15 Ω -cm n^- collector region (10 μ) used for these particular devices in an attempt to observe the influence of the n^- region thickness on the device performance.

Table III

Typical parameters of experimental devices

Run	No. of Good Devices	Junction Depth Base	Junction Depth Emitter	f_t 1 a 20 V	C_{ob} 70 V	B V_{CBO} 1 ma	B V_{CEO} 50 ma	hFE 1 a	hFE 5 a
		μ		Mc	pf	V	V		
8	14	1.8	1.0	430	45	170	150	20	10
9A	3	2.0	1.3	400	50	85	-	-	-
9B	2	1.9	1.1	460	44	100	-	-	-
10	4	2.2	1.2	360	45	200	150	65	10
12	6	1.8	1.0	460	45	160	140	75	10
14	11	1.8	1.0	380	100	105	85	23	18
D2A	5	3.2	2.0	270	35	200	150	35	20
D2B	5	3.1	2.0	390	40	150	100	80	65
16A	7	1.9	1.0	260	45	200	150	10	10
16B	4	1.8	1.0	480	70	140	110	50	35
D4	12	2.7	1.8	430	50	190	180	80	30
D5A	5	2.9	1.8	320	40	200	200	30	15
D5B	6	3.0	1.8	230	80	160	120	20	15

4.5.2 Thermal Resistance Measurement and Hot Spot Detection

Thermal resistance is measured in the circuit of Fig. 12. A pulse of emitter current (usually 1 amp) is applied of sufficient length for the transistor to reach thermal equilibrium. The pulse is then cut off, and the emitter-base junction voltage V_{EB} is observed while a small measuring current of 10 ma is flowing. The junction voltage has a temperature coefficient at this current of 2.3 mv per °C, and can hence be used as a thermometer to measure internal temperature rise. The main features of the waveform observed are shown in the figure. When the current pulse is applied, $|V_{EB}|$ immediately increases owing to the higher forward drop required at the larger current. As the device heats, $|V_{EB}|$ decreases until thermal equilibrium is reached, because a smaller junction voltage is required to sustain a given current at higher temperature. When the current is cut off, another jump in V_{EB} occurs, followed by a slow change back to the original value. The magnitude of this change is proportional to the internal temperature attained during the pulse.

The development of a hot spot is indicated by a sharp spike appearing on the trailing edge of the V_{EB} pulse (see Fig. 12), the amplitude of this spike increasing rapidly as the power ($I_E V_C$) is raised beyond the critical point. At the same time, a "step" in the waveform during the pulse often appears, as shown slightly exaggerated in the figure. This step marks the beginning of the hot spot, and the spike on the trailing edge is the effect of thermally generated carriers from the hot spot flowing out through the base at the termination of the high current pulse. If the power is raised slightly from this point, the transistor enters the "second breakdown" condition and may be destroyed without suitable protective circuitry.

The formation of a hot spot is a consequence of lateral thermal instability as discussed in section 4.3. The resistive layer and emitter resistor structures proposed there are intended to substantially raise the power level at which instability occurs, and thus increase the power handling capacity of the transistor.

The transistors of Table III have thermal resistances measured by the above technique (at a 20 watt level) of from 1.4 to 2.0 °C/watt. Similar values were obtained on units mounted on the TO-3 diamond base package and on the new package described in section 4.4. When contacting methods have been improved so that thicker aluminum can be used, an improvement of the order of 30% is expected in thermal resistance.

Hot spots are typically observed to form at collector voltages of between 30 and 40 volts at an emitter current I_E of 1 amp, at 50 volts for I_E = 0.5a, and at 15 volts for I_E = 4a. At bias levels slightly higher than these, secondary breakdown occurs. If this region is to be avoided, the power output when operating at 50% efficiency would be restricted to 20-30 watts. It is evident that a minimum improvement of a factor of two is necessary; the resistive layer and emitter resistor structures of section 4.3 should provide considerably greater improvement.

4.5.3 Small-signal parameter measurements

Measurement of small-signal high-frequency properties is performed on a General Radio Transfer Function and Immittance Bridge. Since the impedance level of the device in the vicinity of the desired operating frequency (150 Mc) is low (5 to 10 ohms) compared to the characteristic impedance of the bridge (50 ohms), best accuracy is obtained by measuring quantities involving open-circuit rather than short-circuit terminations.

It has been found convenient to measure the common-emitter open-circuit impedance (z) parameters, and correct for the presence of lead inductance by subtracting the impedances measured on a shorted package. To obtain the f_t frequency, the short-circuit current gain h_{21} is calculated from the corrected impedance using the standard relation $h_{21} = -z_{21}/z_{22}$. The frequency f_t is the magnitude of this quantity multiplied by the frequency of measurement. The f_t frequencies reported in Table III are obtained in this manner from measurements made at 160 mc. This procedure is thought to be more accurate than that given in the first quarterly report, where h_{21} is measured directly and corrections made based on an assumed frequency dependence.

Table IV shows common-emitter z parameters on a typical device from run 16B, measured at 160 mc and a bias of 1 amp, 20 volts, with corrections made for lead inductance. A measure of the inherent gain of the device is given by Mason's U function[7], which is the power gain in a circuit where the transistor is neutralized by a lossless network, and is given by

$$U = \frac{|z_{21} - z_{12}|^2}{4\,[\mathrm{Re}(z_{11})\,\mathrm{Re}(z_{22}) - \mathrm{Re}(z_{12})\,\mathrm{Re}(z_{21})]} \qquad (60)$$

Inserting the values from Table IV results in U = 10.1. Thus the transistor is capable of the order of 10 db power gain at 160 Mc, in accordance with the requirements (this figure refers to small-signal conditions only). It is generally assumed that U varies as $1/f^2$ in the upper frequency range. On that basis, the frequency at which U = 1, termed the maximum frequency of oscillation f_{max}, is $\sqrt{10.1} \times 160$ Mc $\simeq$ 510 Mc.

---

7. S. J. Mason, "Power Gain in Feedback Amplifiers," IRE Trans. on Circuit Theory, CT-4, 20 (1954).

Table IV

Typical common-emitter z parameters at 160 Mc, 1 a, 20 V

z_{11}	2.2 + j 4 Ω
z_{12}	1.0 + j 0 Ω
z_{21}	6.0 + j 13 Ω
z_{22}	4.9 - j 1.5 Ω

Figure 13 is a tentative small-signal equivalent circuit which is thought to represent the transistor in the 150 Mc range. The elements C_{bg} and C_{cg} are about 7 pf and 10 pf respectively, and represent capacitances to ground of the transistor and mounting jig in the grounded emitter connection. These capacitances are used to estimate measurement errors caused by finite terminating impedances. The inductances L_b and L_e are each about 10 nhy; roughly half of this is in the mounting jig and half in the package (this refers to the TO-3 package; the inductance of the stud-mounted package has not yet been accurately determined). The remaining elements in Fig. 13 are estimated to be as follows at an operating point of 1 amp, 20 volts:

$r_b = 4\ \Omega$

$r_c = 2\ \Omega$

$C_1 = 20$ pf

$C_2 = 50$ pf

$\alpha = 1/(1 + j\, f/f_t)$ $\quad f_t = 480$ Mc

The capacitance C_2 is due to that portion of the collector-base junction directly under the base contact and in regions where there is no emitter; C_1 is the remaining collector junction capacitance. These values are

tentative; to establish them accurately would require many more measurements over a wide frequency range.

4.5.4 Oscillator Power Output

Some preliminary experiments to determine the rf power output capability of the device have been undertaken. Fig. 14 shows a simple circuit employing coaxial elements for the 150 Mc frequency range. Small capacitors C are used to tune out the inductance of the emitter and base leads. The circuit is a common-collector configuration, in which the feedback takes place through the low impedance of the emitter-base junction. In such a circuit an inductive impedance is connected from base to ground, a negative resistance is seen at the emitter terminal, and oscillation can be sustained in a suitable load circuit. The required inductance is provided by a shorted length of 50 ohm coaxial line less than one-quarter wavelength long. The load circuit is provided by a line about one-half wavelength long with a 50 ohm load connected in such a way that the effective load seen at the transistor terminals can be varied over a wide range.

The initial results obtained with the devices tabulated in Table III have not been encouraging. The best devices were generally those with the highest cutoff frequency, but even these delivered only about 1 watt at 150 Mc at an operating bias of I_c = 600 Ma, V_c = 35 volts. Higher current resulted in lower power. The power increased with voltage, but 35 to 40 volts was the limit imposed by the thermal instability discussed in Section 4.3.

Similar results to those quoted above were obtained with a lumped-element circuit analogous to Fig. 14. Since it is possible that a different configuration may be more favorable, other circuit arrangements are presently being investigated.

There are two probable reasons for the low power output at 150 Mc. First of all, the thickness of the evaporated aluminum contacts on the devices tested is only about 0.3 μ. (Problems encountered in metallizing are discussed in Section 4.2.) This thickness is almost a factor of 10 times smaller than that desirable for low transverse rf voltage drops, and the result is probably that only a small fraction of the device area is effectove. The second reason is that most of the region under the relatively wide backbone will be virtually isolated from the base contact because of the severe emission crowding existing under large signal conditions. The charging current flowing in the collector junction capacity in this region will be largely drawn from the emitter, and the phase relationships involved result in a net power dissipation. Thus most of the power generated in the remaining part of the transistors may be lost in the region under the backbone. The structure proposed in Section 4.3.7 and presently being made will obviously eliminate this effect, since no emitter layer exists under the backbone. It is believed that this structure with suitably thick contacts will result in an order of magnitude increase in power output, and incorporation of the stabilizing resistors to allow operating with higher temperature rises will further improve the performance.

5. CONCLUSIONS

It is expected that power limitations due to lateral thermal instability can be overcome by means of the structure with stabilizing emitter resistors described in Section 4.3.7. The small-signal properties of the device are generally as expected, but the large-signal performance at 150 Mc is very poor. This performance can probably be greatly improved by employing much thicker aluminum contacts, and by omitting the emitter diffusion under the backbone.

6. PROGRAM FOR NEXT QUARTER

Emphasis will be placed on producing devices with stabilizing emitter resistors, and much thicker aluminum contacts. These devices have no emitter diffusion under the backbone. At the same time, a more intensive study of the conditions obtaining under large-signal high-frequency operation will be undertaken. If the power output at 160 Mc shows the expected improvement, preparations will be made for producing the 200 devices called for in this contract.

7. PERSONNEL

Engineering time expended during the period covered by this report is as follows:

Senior Scientists

R. Scarlett (Chief Investigator)	179 Hours
A. Goetzberger	123 Hours
R. Gereth	37 Hours
H. Queisser	111 Hours
W. Schroen	177 Hours
H. Strack	8 Hours
M. Heynes	56 Hours

Associate Scientists

R. Finch	341 Hours
L. Johnson	292 Hours
N. Zetterquist	403 Hours
W. Hooper	266 Hours
R. Regehr	48 Hours
T. Swanson	224 Hours

APPENDIX A

Evaluation of Resistive Layers

Consider the resistive layer sample shown in Fig. A. 1. The region of interest is the middle n^- layer, of g mhos per sq cm conductance.

The current I flows out from the contact on the n^+ surface. At a radial distance r from the contact, the current I_1 flowing in the surface layer is

$$I_1 = - \frac{2\pi r}{R_s} \frac{d\,V(r)}{dr} \tag{A.1}$$

where V(r) is the potential at r of the surface layer with respect to the substrate, and R_s is the sheet resistance of the n^+ layer. The current I_1 is less than I because some of the current has been lost to the substrate through the resistive layer between 0 and r. The current lost at r through an interval dr is

$$dI_1 = - 2\pi r\, g\, dr\, V(r) \tag{A.2}$$

Equating the divergence of I_1 in Eq. (A. 1) to Eq. (A. 2) gives

$$d\,I_1 = \frac{2\pi}{R_s} \left[\frac{d\,V(r)}{dr} + r \frac{d^2 V(r)}{dr^2} \right] dr = 2\pi r g\, dr\, V(r) \tag{A.3}$$

which results in the following equation for the potential V(r)

$$\frac{d^2 V(r)}{dr^2} + \frac{1}{r} \frac{d\,V(r)}{dr} = g\, R_s\, V(r) \tag{A.4}$$

By choice of a scale factor $x = r\sqrt{g R_s}$ Eq. (A. 4) is identical to

$$\frac{d^2V}{dx^2} + \frac{1}{x}\frac{dV}{dx} = V \qquad \text{(A. 5)}$$

The appropriate solution of Eq. (A. 5) is a Hankel function of x, $iH_o^{(1)}(ix)$, with boundary conditions $iH_o^{(1)}(ix) = 0$ at $x = \infty$ and $iH_o^{(1)}(ix) = \infty$ at $x = 0$. Values of this function are available in standard mathematical tables. The potential V(r) is found by probing in the vicinity of the current contact along a radius r. The measured values of V(r) vs r for a typical sample are plotted on a log-log scale shown in Figure A. 1.

The Hankel function $iH_o^{(1)}(ix)$ is also plotted on the same scale from x = 0. 1 to 10. The experimental points are fitted to the Hankel function by translation only, and r is found on the V(r) vs r plot which corresponds to x = 1 on the $iH_o^{(1)}(ix)$ vs x plot. If this value of r is denoted by r_1, then

$$g = \frac{1}{r_1^2 R_s} \qquad \text{(A. 6)}$$

An estimated value of g for the data plotted in the figure is 1 15 mho cm^{-2}, from $r_1 = 260\,\mu$ and $R_s = 13\,\Omega$. This is an R_r (see Eq. 57) of about 10^{-2} ohm-cm^2. The sheet resistance R_s is obtained from data taken close to the current probe where the potential varies as $-(IR_s/2\pi)\ln r$.

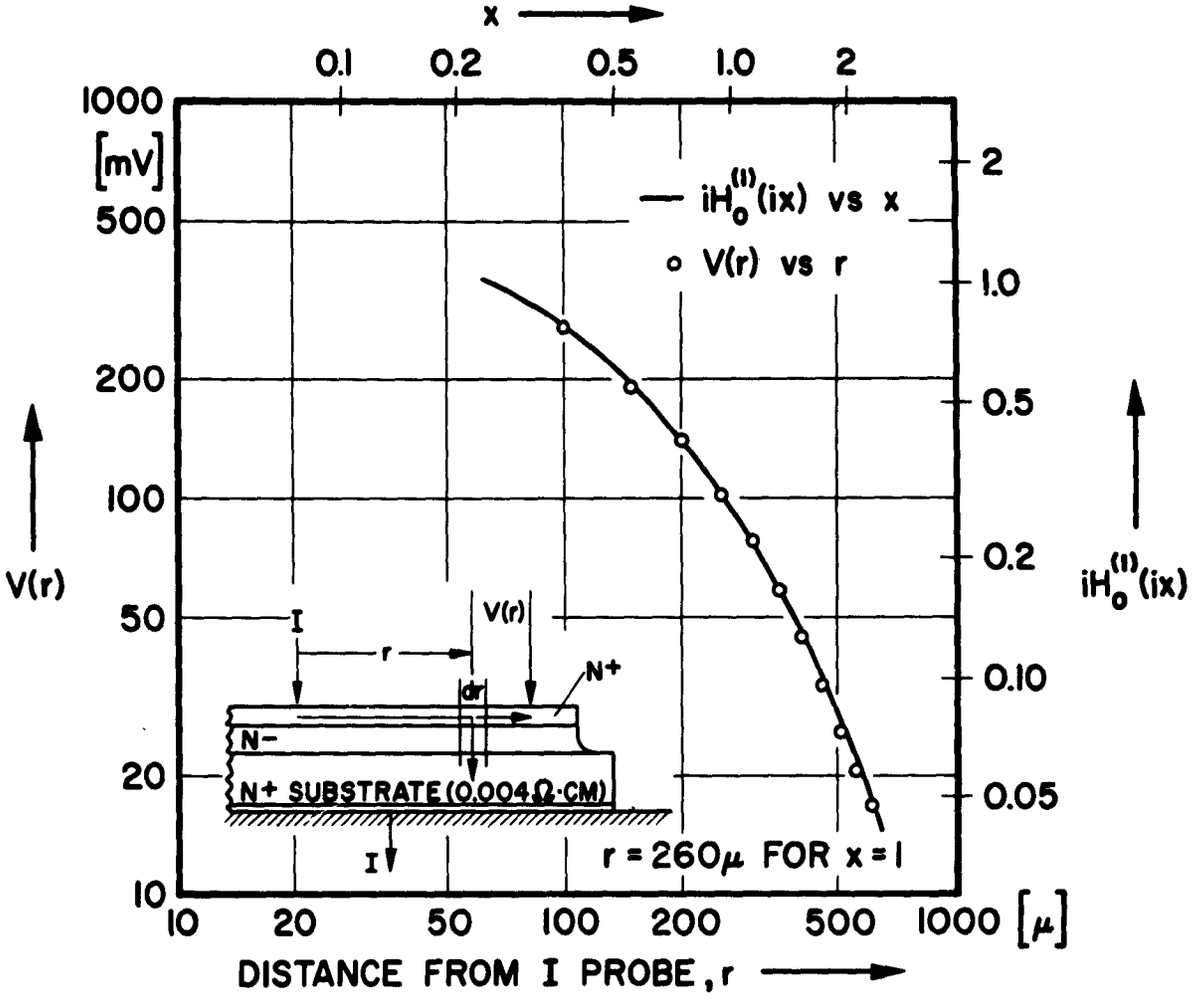


Figure A. 1

Measure of resistive layer

1-16-63
50508

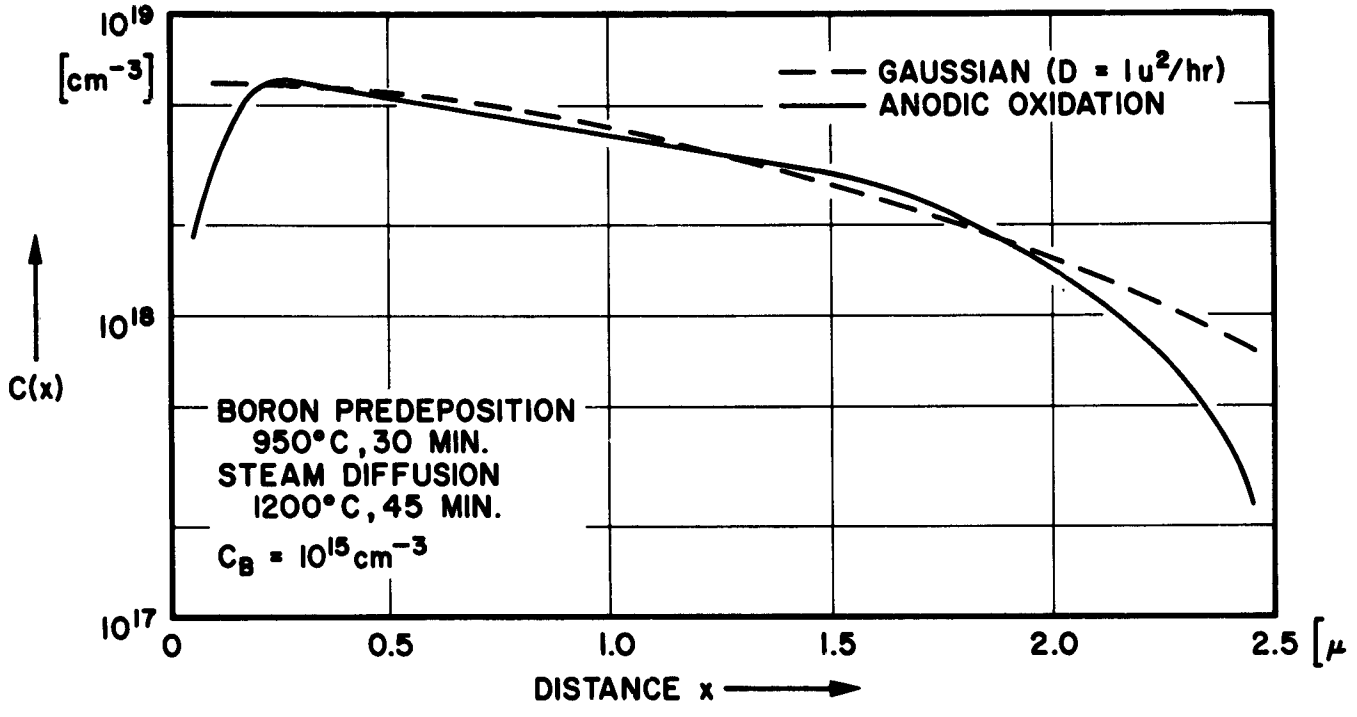


Figure 1

Boron diffusion profile

1-17-63
50512

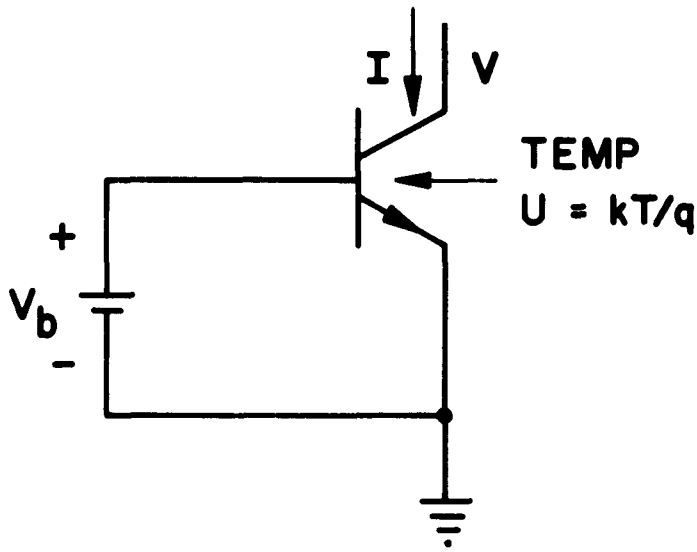


Figure 2

The transistor as a thermistor

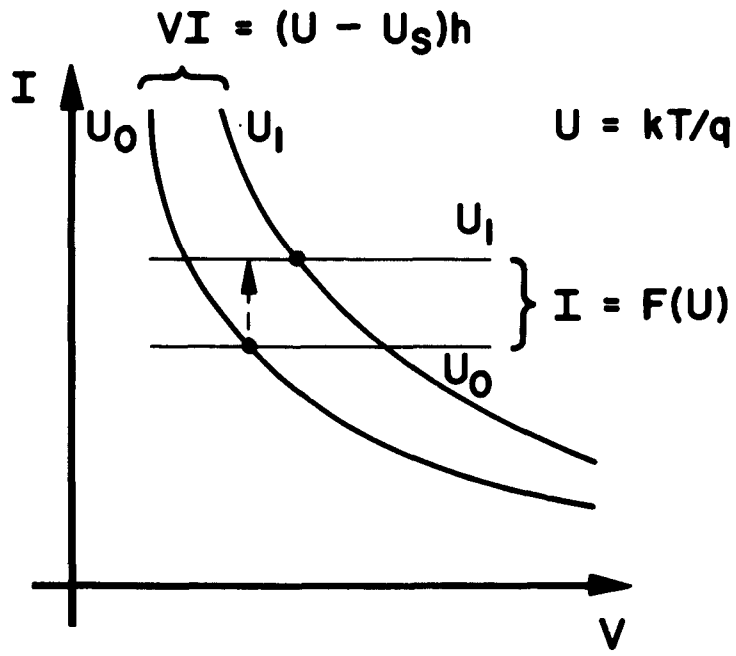


Figure 3

Transistor power-temperature-current relations

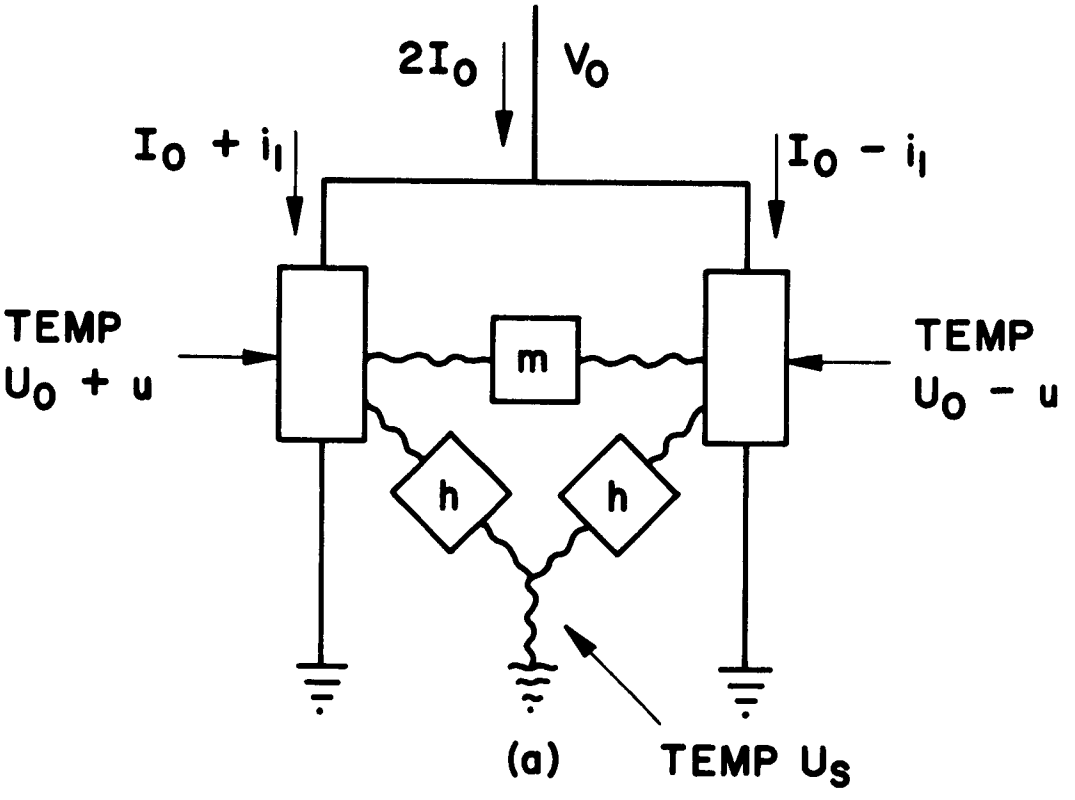


Figure 4

Two transistors in parallel

1-17-63
50510

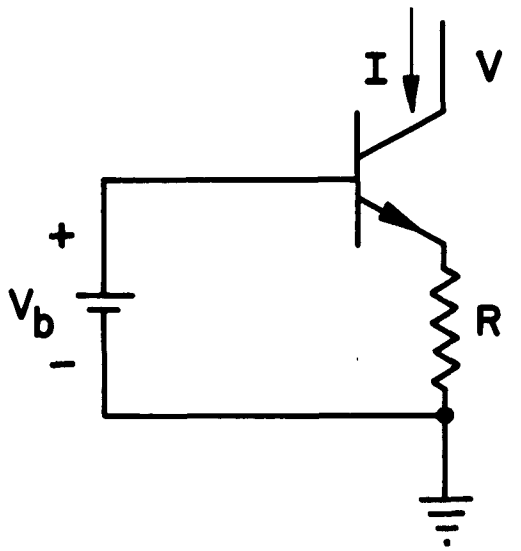


Figure 5

Transistor with emitter resistor

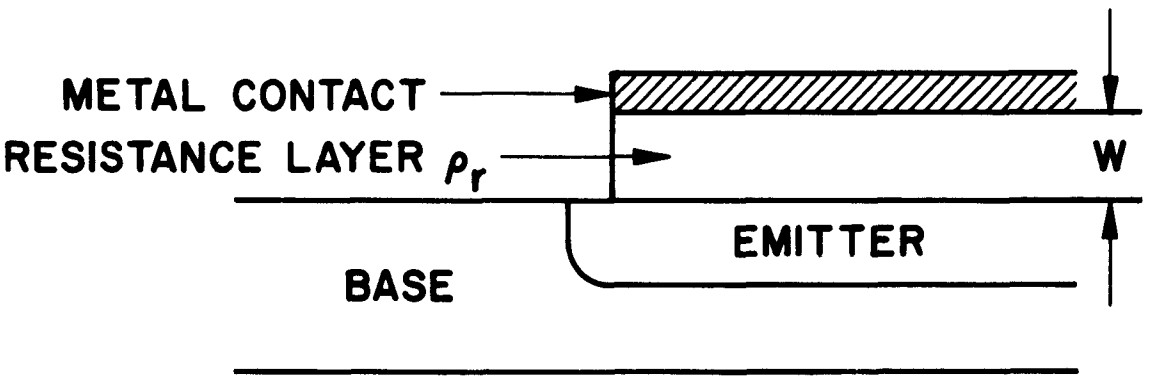


Figure 6

Distributed resistive emitter layer

Figure 7

Power transistor with epitaxial resistive layer over the emitter area (light). Dark strips are base fingers

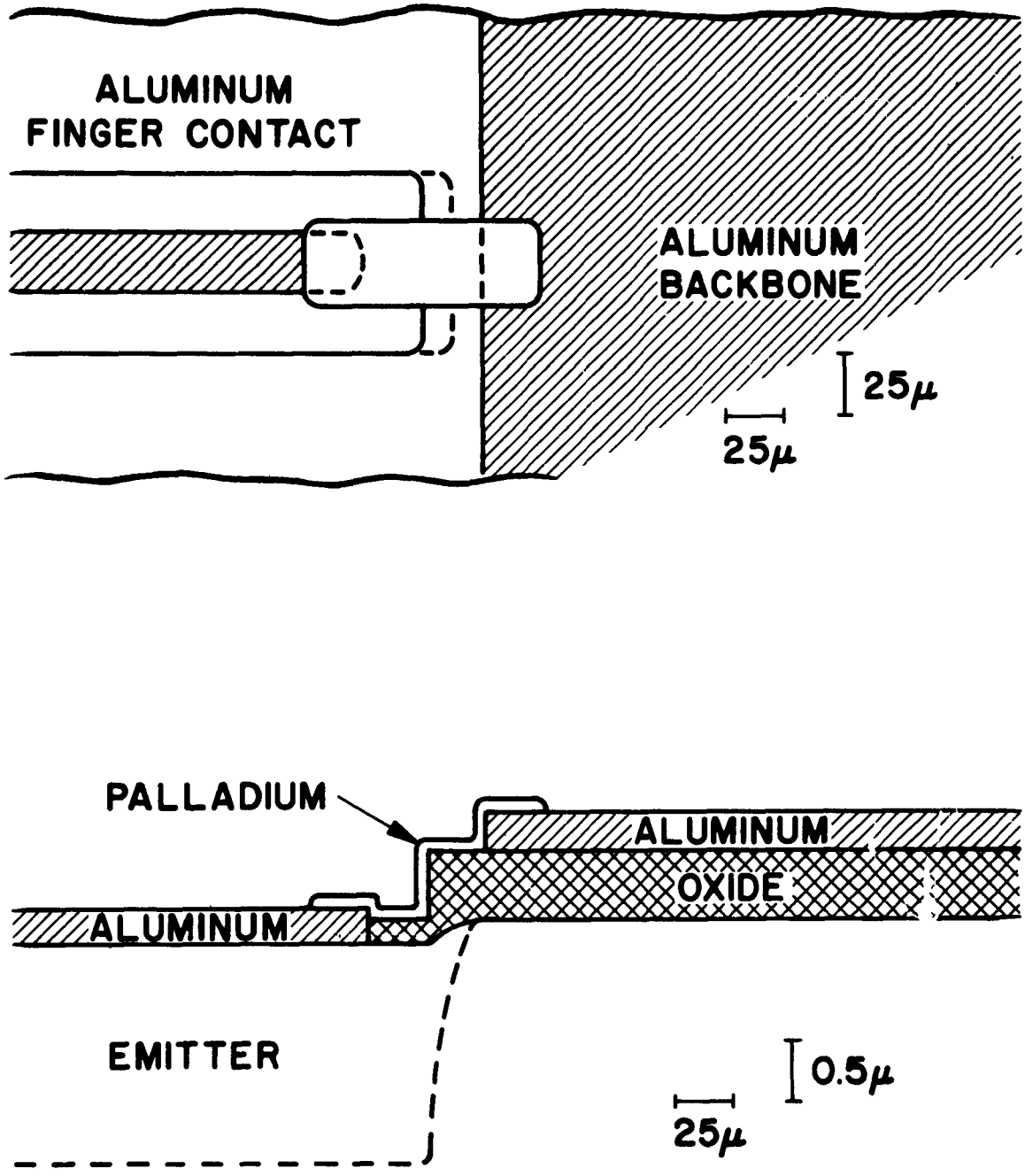


Figure 8

Palladium resistor in series with emitter finger

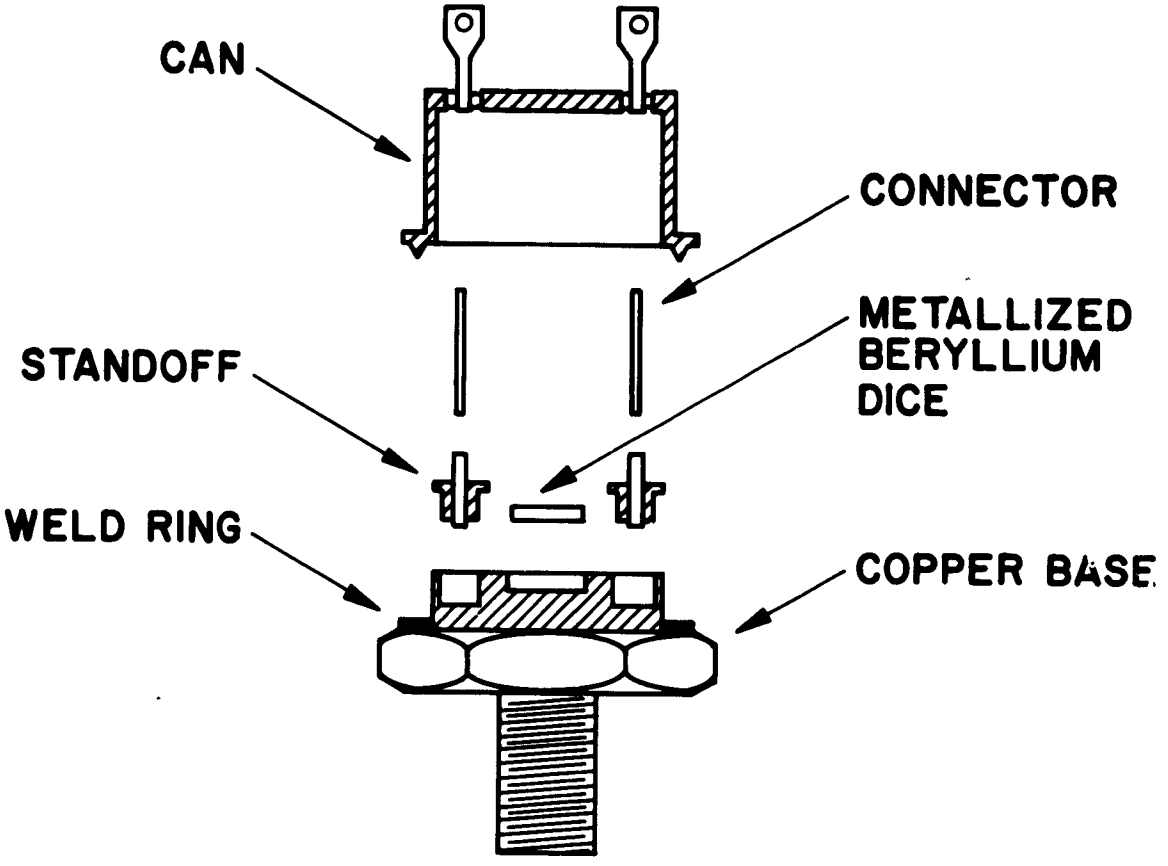


Figure 9

Package assembly

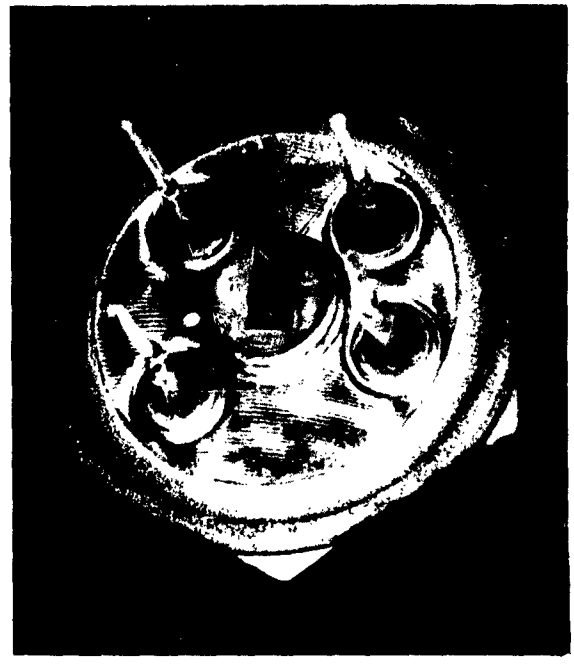


Figure 10

Package without can

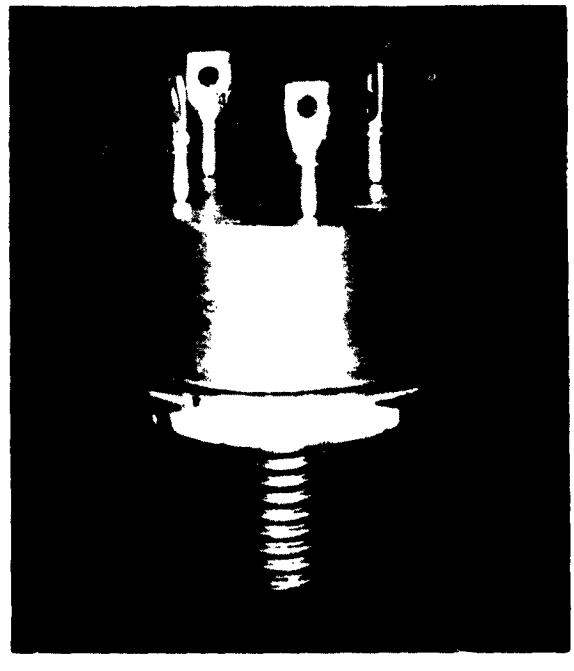
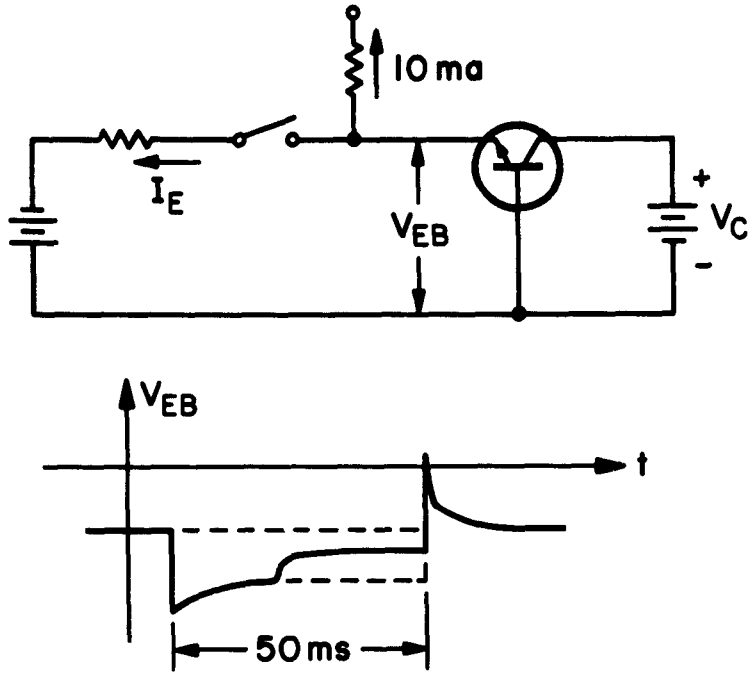


Figure 11

Complete package



EMITTER-BASE VOLTAGE
DURING HOT SPOT FORMATION

Figure 12

Measurement of thermal resistance and hot spot development

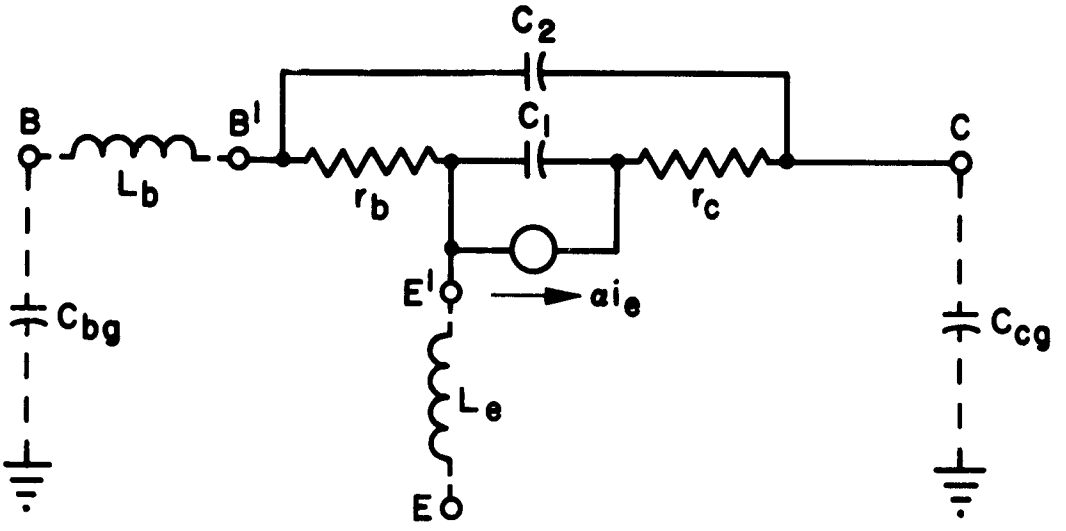
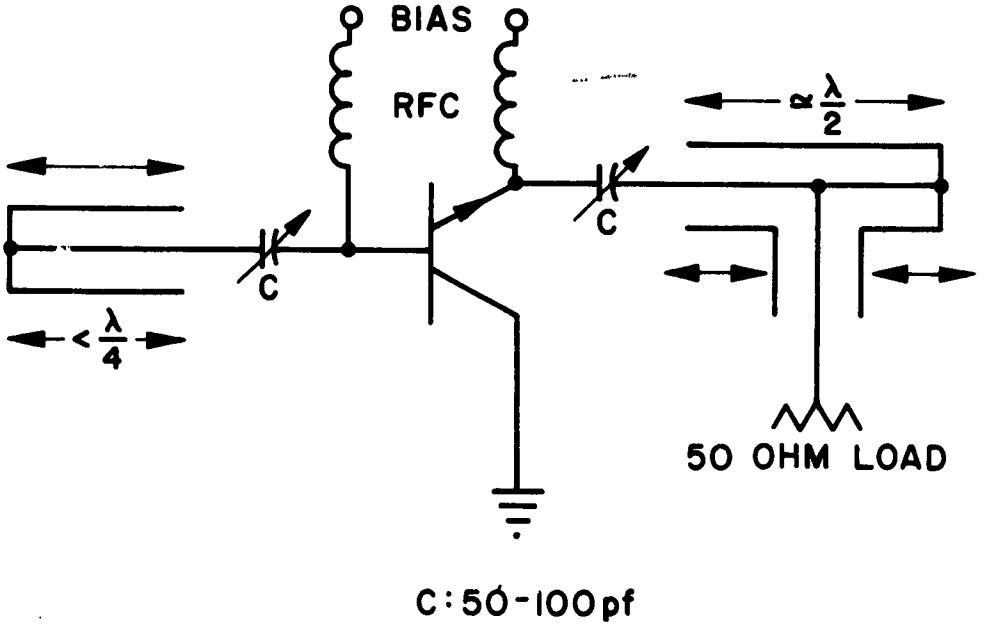


Figure 13

Tentative equivalent circuit



C: 50-100pf

Figure 14

Experimental oscillator circuit

1-21-63
50518

AD______________

Shockley Transistor, Unit of Clevite Transistor, Palo Alto, Calif.

VHF SILICON POWER TRANSISTOR, Ed. R. M. Scarlett

Report covering 10-1-62 to 1-1-63, 61 pps, incl. illus.
Second Quarterly Report (Contract DA 36-039 SC 90837)

The continued development of the 50 watt VHF silicon power transistor in the areas of diffusion, metallizing and packaging is described. The theory of lateral thermal instability is discussed. This instability is fundamental to all transistors, and leads to the development of hot spots and consequent secondary breakdown. It severely limits the power capability of large-area devices. Means are proposed to substantially raise the power level at which the instability occurs. Initial experiments in making stabilized devices employing either epitaxially grown resistive emitter layers, or lumped emitter resistors are reported.

Experimental devices show the expected small-signal properties ($f_t \simeq f_{max} \simeq 450$ Mc), but the large-signal performance is still poor due to insufficiently thick metal contacts and the influence of the wide backbone region.

Unclassified

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2. Transistors - Power

I. Title: VHF Power Transistor

II. Scarlett, R.

III. U.S. Army Signal Research Ft. Monmouth, N.J.

IV. Contract DA 36-039-SC 90836

Uniterms:

Transistors
Very High Frequency
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